Eur. Phys. J. B **42**, 113–117 (2004)
DOI: 10.1140/epjb/e2004-00362-y

THE EUROPEAN PHYSICAL JOURNAL B

An analytical study of substrate current in submicron MOS devices

G. Vaidyanaath G.[1,a] and A.K. Singh[2]

[1] No. 66/3, ASIC, Texas Instruments, Bagmane Tech Park, C.V. Raman Nagar Post, Byrasandra, Bangalore, 560093 Karnataka, India
[2] Birla Institute of Technology and Science, Pilani, 333031 Rajasthan, India

Received 23 April 2004 / Received in final form 27 September 2004
Published online 26 November 2004 –

Abstract. In the present communication we have tried to study the substrate current behavior in the submicron devices after solving the second order differential equation using appropriate boundary conditions. Simple and accurate models for maximum lateral field, drain saturation voltage and for ionization length have been developed. The simulation result of ionization length shows a good match with the known result. Analysis also shows that dominant contributor to the error in the ionization length is not only because of the excess saturated voltage but also due to the channel length and the gate to source voltage. For sub-micron devices the saturation region shifts towards the source for higher drain voltage and larger gate oxide thickness.

PACS. 85.30.De Semiconductor-device characterization, design, and modeling – 85.30.Tv Field effect devices

1 Introduction

In short-channel MOS transistor the velocity saturation region length (LVSR), where impact ionization occurs and carrier velocity saturates, is an important parameter to study because it is related to the device degradation and device lifetime [1–4]. This region governs the drain-breakdown voltage [5,6] and hot electron generation [7,8]. In a short channel device due to high electric field, a measurable substrate current flows due to electron-hole pair generation near the drain [9]. The substrate current is an important parameter in measuring and investigating the impact ionization phenomenon in scaled MOSFET's [10]. The substrate current is highly sensitive to device dimensions, channel doping and temperature. Its accurate prediction provides vital information in both ensuring reliability of the devices and analyzing circuit level reliability in VLSI/ULSI design. Several analytical models for substrate current behavior have been reported [11–16] but these models are not very simple and having many fitting parameters.

In the present work we have derived the relations for ionization length and substrate current in sub-micron devices. These relations were solved with the help of models developed by us. Our simulated results show an excellent match with the experimental as well as established findings. In Sub micron devices the LVSR length is not only affected by excess drain voltage beyond saturation but also due to gate oxide thickness, channel length and gate to source voltage. The saturation region shifts towards the source as one increases the drain voltage. The effect of the gate voltage on the saturation length region is more pronounced as one scales down the length

2 Model formulation

Consider an n-channel MOSFET of length L, operating in the saturation region. The coordinate system chosen is Y-axis (perpendicular to the channel length) and X-axis (along the channel length). The substrate current in an n-channel MOSFET is given by [13]:

$$I_{sub} = I_d A_i \int_0^x e^{-B_i/E_i(x)} dx \tag{1}$$

where I_d is drain saturation current, A_i and B_i are the ionization constants, $x = (L - l_d)$ gives the velocity saturated channel region.

Assuming the electric field $E(x)$ along the channel is independent of the junction depth and varies linearly from zero to E_{sat} [15], one has,

$$\left.\frac{dE(x)}{dx}\right|_{x=L-l_d} = \frac{E_{sat}}{L - l_d} \tag{2}$$

where E_{sat} is the minimum electric field for velocity saturation. Solving the second order differential equation [18] for the boundary condition (2), the channel

[a] e-mail: gokul_vaidyanaath@yahoo.co.in

potential $V(x)$ is given by:

$$V(x) = \frac{\lambda}{L - l_d}\left[V_{dsat}\mathrm{Sinh}\left(\frac{x-(L-l_d)}{\lambda}\right) + \lambda E_{sat}\mathrm{Cosh}\left(\frac{x-(L-l_d)}{\lambda}\right)\right] \quad (3)$$

where $\lambda = \sqrt{\frac{\varepsilon_{si} X_j t_{ox}}{\varepsilon_{ox}}}$ is characteristics length.

Differentiating (3) w.r.to x and after simplification, the electric field along the channel is:

$$E(x) = \sqrt{\left[\frac{V^2(x)}{\lambda^2} + \frac{\lambda_2}{(L-l_d)^2}\left(\frac{V_{dsat}^2}{\lambda^2} - E^2{}_{sat}\right)\right]}. \quad (4)$$

Using relations (1) and (4) and rearranging the terms we have:

$$I_{sub} = I_d A_i \lambda \int_{E_{sat}}^{E_m} \frac{e^{-B_i/E_i(x)}}{\sqrt{\left[E^2(x) - d^2\right]}} dE(x) \quad (5)$$

where $d^2 = (\frac{\lambda}{L-l_d})^2[(\frac{V_{dsat}}{\lambda})^2 - E^2{}_{sat}]$ and E_m is the maximum electric field at $x = L$.

Solving the integral (5), we get

$$I_{sub} = \left(\frac{I_d A_i \lambda}{B_i}\right)\left[E_m e^{-B_i/E_m} - \frac{1}{2}\left(1 - \left(\frac{\lambda}{L-l_d}\right)^2\right) E_{sat} e^{-B_i/E_{sat}}\right]. \quad (6)$$

Here, we have modeled the maximum electric field (E_m) empirically as

$$E_m = \delta\left(\frac{V_{ds} - V_{dsat}}{l_d}\right). \quad (7)$$

where $\delta(< 1)$ is a fitting parameter, which takes care of temperature variation of V_{dsat} and voltage drop across the channel.

For $E_m \gg E_{sat}$; equation (6) reduces to

$$I_{sub} \approx \left(\frac{I_d A_i \lambda}{B_i}\right) e^{-\frac{B_i}{E_m}}. \quad (8)$$

To know the value of A_i at given B_i we have used the empirical formula given by Seah et al. [17] as:

$$A_i = \beta_1 \exp\left(-\beta_2 V g s\right) \quad (9)$$

where β_1 and β_2 are technology dependent parameters.

Expression (8) is similar to expression given in reference [13]. The first term of equation (6) shows the exponential dependence on l_d whereas second term shows that the substrate current is inversely proportional to l_d. Since, the first term is dominating over second, therefore, it is concluded that a little error in the calculation of ionization length can translate into a larger error in I_{sub}. l_d is dependent on the channel length L, characteristics length λ and excess drain voltage beyond saturation (i.e. $V_{ds} - V_{dsat}$). Following the same procedure as mentioned in the reference [16], the expression for l_d is derived as:

$$l_d = \lambda \ln\left[\frac{(b+c) + \sqrt{\left[b^2 + 2bc + c^2(a^2-1) + a^2\right]}}{a(c+1)}\right] \quad (10)$$

where $b = \frac{(V_{ds} - V_{dsat})}{\lambda}$; $a = (\frac{\lambda}{L-l_d})$ and $c = (\frac{V_{dsat}}{\lambda E_{sat}})$.

From equation (10) it is clear that the term 'a' also depends upon l_d, thus this equation is transcendental in nature. In the present work, for a given t_{ox} and X_j, an approximation is used for the term a, which is given by

$$a = \frac{\lambda}{L - \eta L(V_{ds} - V_{dsat})} \quad (11)$$

where η (unit 1/volt) is a fitting parameter. To get the substrate current we need V_{dsat}, which is modeled as:

$$V_{dsat} = \left[L E_c\left(\sqrt{\left(1 + \frac{\gamma V_{gs} - \beta V_{th}}{L E_c^{\alpha}}\right)}\right) - 1\right] \quad (12)$$

where V_{gs} is gate to source voltage and γ, β and α are fitting parameters. The fitting parameter β is introduced to account the threshold voltage reduction due to DIBL effect, temperature variation and Channel length Scaling. The parameter γ is related to fabrication error. According to Arora et al. [13] α is a term involving body effect.

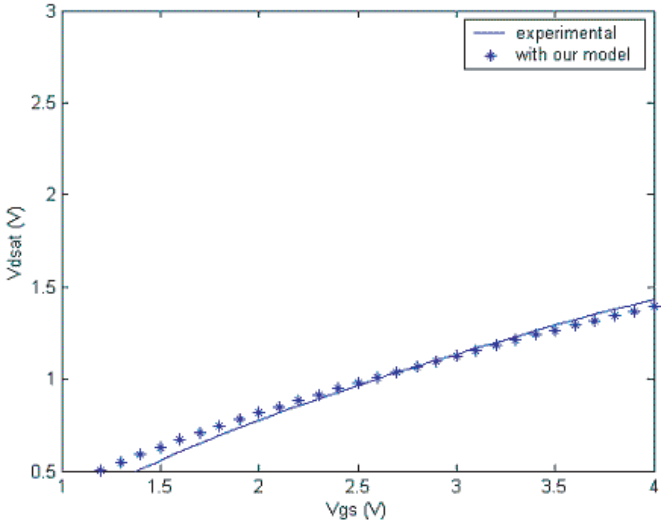

Fig. 1. Measured and simulated V_{dsat} values as a function of gate voltage V_{gs}.

3 Numerical result

The measured V_{dsat} for a given channel length ($L = 0.25\ \mu$m) as a function of V_{gs} is shown in Figure 1. These

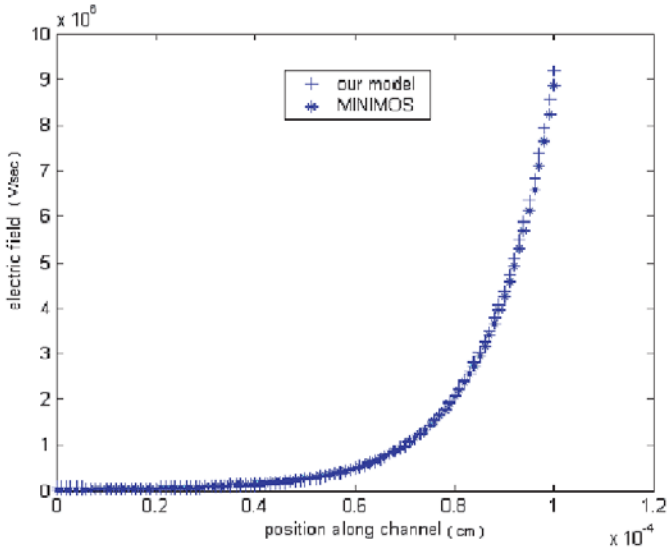

Fig. 2. Variation of lateral electric field with the distance along channel. Data in markers (*) are MINIMOS simulation and curves are analytical results (Eqs. (4) and (12)).

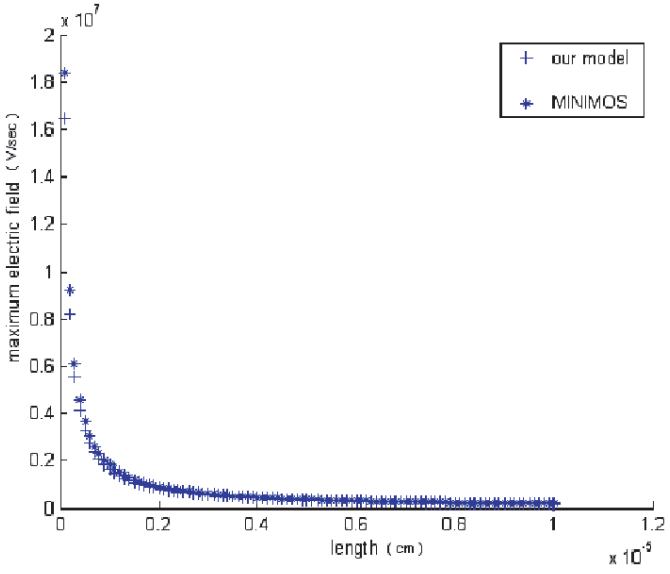

Fig. 3. Plot of maximum lateral field with ionization length l_d.

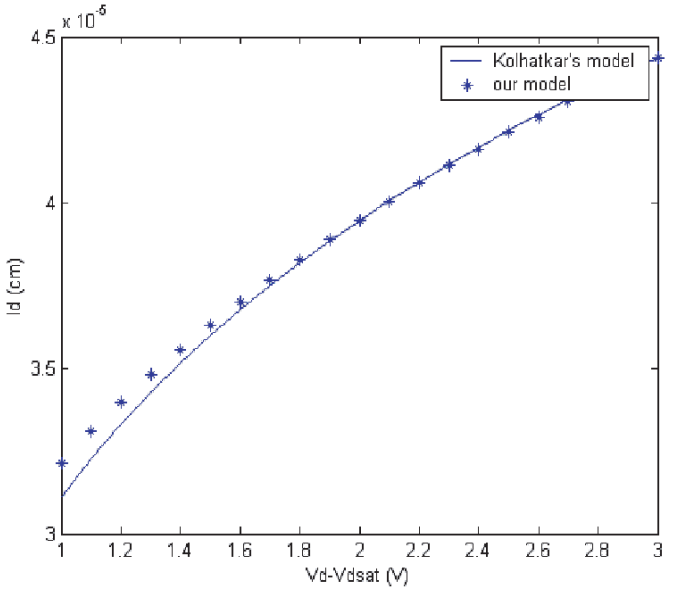

Fig. 4. Plot of velocity saturation region length as a function of excess drain voltage beyond saturation. The symbol (*) gives Kolhatkar model's result and curve represents analytical results.

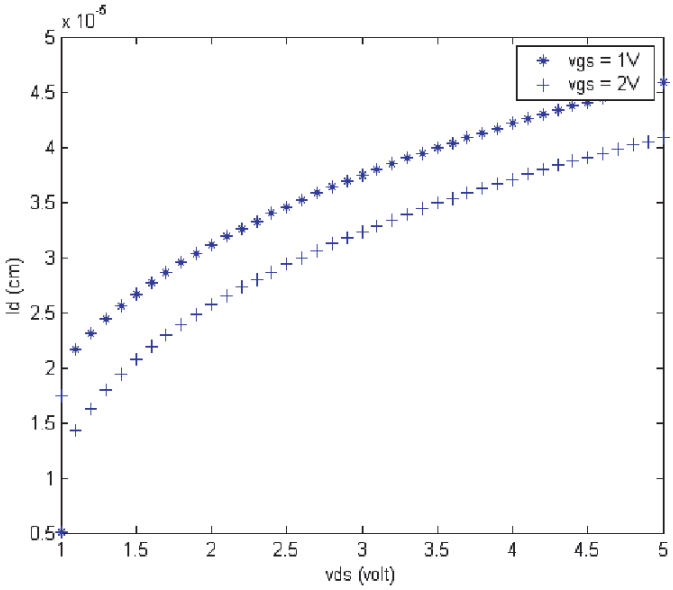

Fig. 5. Velocity saturation region length variation with V_{ds} for $V_{gs} = 1$ V and $V_{gs} = 2$ V.

experimental V_{dsat} points are curve fitted to equation (11) to extract the values of parameters γ and β. The parameters are chosen according to Arora et al. [13].

With the extracted values of γ and β, we have plotted a graph for lateral field versus distance along the channel as shown in Figure 2. Our simulated result using equations (4) and (12) shows an excellent match with the MINIMOS results.

With the maximum electric field from Figure 2 we have extracted the value of fitting parameter δ. Figure 3 shows a plot of maximum electric field as function of saturation length region. From Figure 3 it is observed that the maximum field graph (calculated by using Eq. (7)) shows a good match with Arora's et al. [13] model.

The simulated results obtained from equation (10) are plotted as a function of $(V_{ds} - V_{dast})$ in Figure 4. The symbol (*) in Figure 4 shows the simulated results of Kolhatkar et al. [16]. By matching the two results the fitting parameter η is obtained.

With extracted values of all the fitting parameters a graph is plotted between saturation length and V_{ds} for two different values of $V_{gs}(= 1\text{ V}, 2\text{ V})$ as shown in Figure 5. The ionization length increases with V_{ds} for a given V_{gs}. This only shows that the saturation length shifts towards the source end. The effect of the gate voltage is to reduce the ionization length for a given V_{ds}.

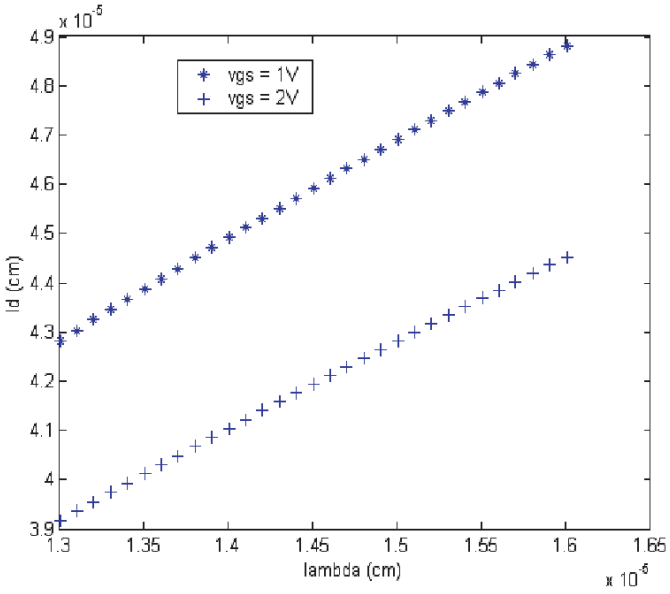

Fig. 6. Variation of ionization length with characteristic length (λ) for $V_{gs} = 1$ V and $V_{gs} = 2$ V.

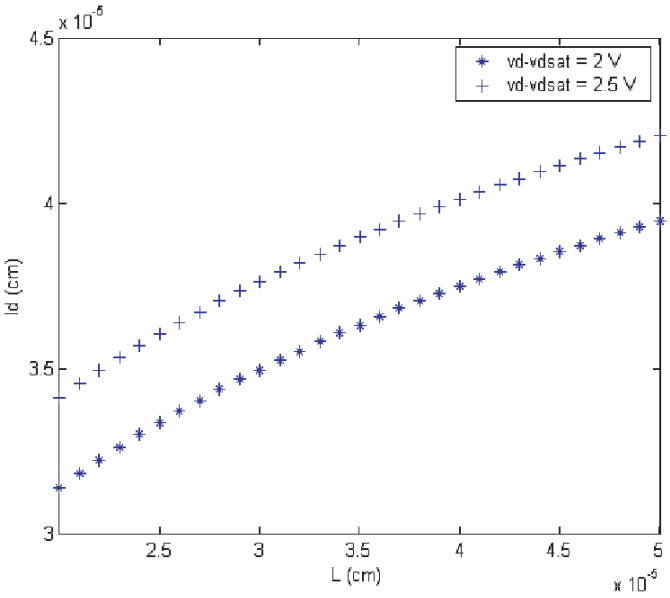

Fig. 7. Plot of channel length dependence of the velocity saturation.

Figure 6 shows a plot of l_d as a function of λ for $V_{gs} = 1$ V and $V_{gs} = 2$ V. The general trend is that the saturation length increases linearly with the oxide thickness for fixed junction depth and channel length. It is also observed that for sub-micron devices the gate voltage has more effect on the saturation length [17].

Variation of saturation length as a function of channel length for $(V_{ds} - V_{dsat}) = 2$ V and $(V_{ds} - V_{dsat}) = 2.5$ V is shown in Figure 7. The general nature of the curve is same as shown by Wang et al. [15]. The observation only reflects the findings of Wang et al. [15] that the change of LVSR

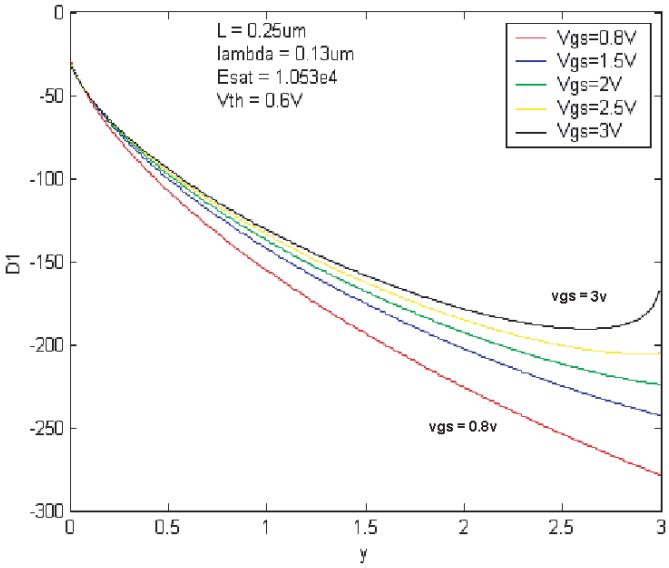

Fig. 8. Gate – bias influence on plots used to compute Ai.

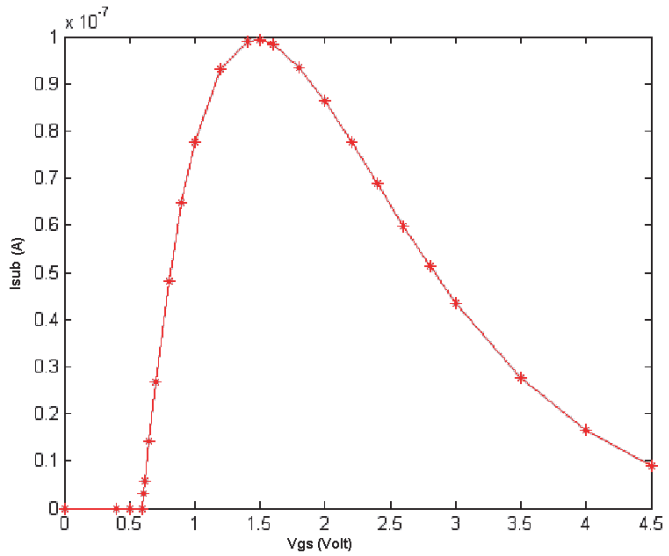

Fig. 9. Substrate current versus gate voltage for n MOSFET with $L = 0.25$ μm, $V_{ds} = 2.5$ V and $V_{sb} = 0$ V.

with channel length is more pronounced for sub-micron devices.

Figure 8 shows the variation of $\ln(I_{sub}/I_d(V_{ds} - V_{dsat}))$ (D1 in Fig. 8) curve as a function of $(1/(V_{ds} - V_{dsat}))$ (y in Fig. 8) for different gate voltages and channel length of 0.25 μm. With the help of this result the parameter A_i is obtained.

A plot of I_{sub} as a function of gate voltage V_{gs} with drain voltage as a parameter is shown in Figure 9 for $L = 0.25$ μm and other parameters are chosen accordingly. As clear from the figure that the substrate current initially increases with $V_{gs}(V_{gs} > V_{th})$ and reaches to its maximum value at a particular gate-source voltage. This increase in substrate current is due to increase in drain-saturation current. As discussed by Arora's et al. [13], a

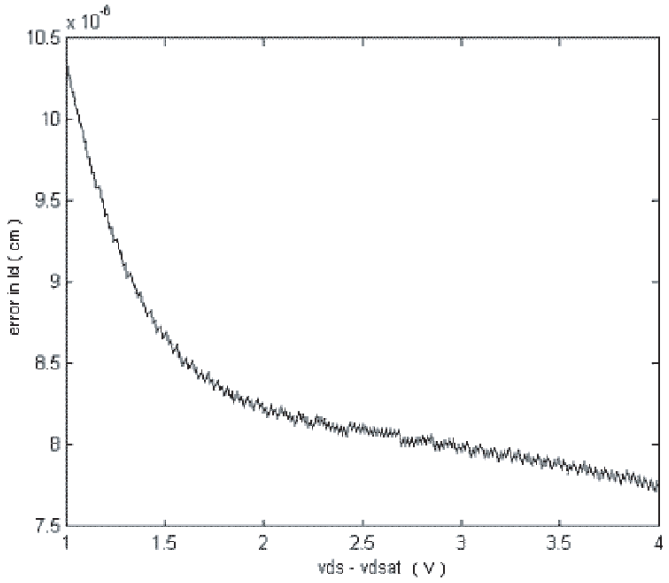

Fig. 10. Plot of error with excess drain voltage beyond saturation.

further increase in V_{gs} will increase the saturation drain voltage (see Eq. (12)), which in turn reduces the maximum electric field, and hence substrate current will reduce. Our simulated result shows a good match with Seah [17] result at lower gate voltage whereas for higher gate voltage a little difference is reported.

We have also solved the transcendental equation (10) without any approximation in a and compared the result with approximated result (Eq. (11)) and error between two results is plotted as a function of $(V_{ds} - V_{dsat})$ as shown in Figure 10. The error reduces with the increase in excess drain voltage beyond saturation. It is also observed that the reported error is very less at a given $(V_{ds} - V_{dsat})$ for the channel length 0.30 μm $\leq L <$ 0.4 μm. So, it is concluded that the approximation given by equation (11) holds good for sub-micron devices.

References

1. E. Takeda, N. Suzuki, An *empirical model for device degradation due to hot carrier injection*; and N. Suzuki, IEEE Trans. Electron Devices Lett. **4**, 111 (1983)
2. C. Hu, S.C. Tams, F.L. Hsu, P.K. Ko, T.Y. Chen, K.W. Ternil, IEEE Trans. Electron. Devices **32**, 375 (1985)
3. W. Weber, C. Werner, A. Schwerin, *Lifetimes and substrate currents in static and dynamic hot-carrier degradation*, IEDM Tech. Dig. (1986), p. 30
4. N. Einspruch, G. Glidenblat, *Hot carrier effect*, Advanced MOS Device Physics, Vol. 18 (VLSI Electronics, Academic, New York, 1989)
5. S.E. Laux, F.H. Gaenssless, IEEE Trans. Electron Devices **34**, 1066 (1987)
6. Hei Wong, Microelectronics Reliability **40**, 3 (2000)
7. H. Wong, Y.C. Cheng, J. Appl. Phys. **74**, 7364 (1993)
8. P. Moens, G. Vandenbosch, G. Groesenken, IEEE Trans. Electron Devices **5**, 623 (2004)
9. K. Lee, M. Shur, T.A. Fjeldly, T. Ytterdal, *Semiconductor Device Modeling for VLSI* (Prentice-Hall, 1993)
10. K. Sonoda, K. Taniguchi, C. Hamaguchi, IEEE Trans. Electron Devices **38**, 2662 (1991)
11. J. Mar, S.S. Li, S.Y. Yu, IEEE Trans. Computer Aided Design **1**, 183 (1982)
12. Y. Chan, P.K. Ko, C. Hu, IEEE Trans. Electron Devices Lett. **6**, 551 (1985)
13. N.D. Arora, M.S. Sharma, IEEE Trans. Electron. Devices **38**, 1392 (1991)
14. K. Takeuchi, M. Fukuma, IEEE Trans. Electron. Devices **41**, 1623 (1994)
15. H. Wang, M.C. Poon, IEEE Trans. Electron Devices **44**, 2033 (1997)
16. J.S. Kolhatkar, A.K. Dutta, IEEE Trans. Electron Devices **47**, 861 (2000)
17. S.H.L. Seah, K.S. Yeo, J.G. Ma, M.A. Do, *Improved prediction of Length/Temperature-Dependent Impact Ionization Induced Body Current Based on an accurate Saturation Drain Voltage model*, Technical Proceedings of the 2000 International Conference on Modeling and Simulation of Microsystems MSM 2000
18. T.A. Fjeldly, M. Shur, IEEE Trans. Electron Devices **40**, 137 (1993)